Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) ~~Integrated~~ An integrated circuit, comprising:

at least one processing unit (PU);

a cache memory (L2_bank) having a plurality of memory modules for caching data;

remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first bank of memory modules to a second bank of memory modules.

2. (currently amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein said cache memory (L2_BANK) is a set-associative cache.

3. (currently amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a programmable permutation function.

4. (currently amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a reduction mapping, wherein the reduction mapping performs the remapping using less output symbols than input symbols.

5. (currently amended) ~~Integrated~~ The integrated circuit according to claim 1, further comprising:

a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and

wherein said remapping means is arranged in series with said Tag RAM unit (TagRAM).

6. (currently amended) ~~Integrated~~ The integrated circuit according to claim 1, further comprising:

a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and

wherein said remapping means is arranged in parallel to said Tag RAM unit (TagRAM).

7. (currently amended) ~~Integrated~~ The integrated circuit according to claim 5, further comprising:

a look up table for marking faulty memory modules.

8. (currently amended) ~~Method~~ A method of cache remapping in an integrated circuit having at least one processing unit (PU); a main memory (MM) for storing ~~data~~ data; and a cache memory (L2_BANK) having a plurality of memory modules for caching data, the method comprising ~~the step of~~:

performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first bank of memory modules to a second bank of memory modules.

9. (new) The integrated circuit according to claim 1, wherein the remapping means is further configured to distribute faulty memory modules evenly over a plurality of banks.

10. (new) The integrated circuit according to claim 1, wherein the remapping means is further configured to perform the unrestricted remapping at a block/line granularity of the memory modules.

11. (new) The integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules from an index to a different index.